Amendments to the Specification:

Please replace paragraph [0030] with the following amended paragraph:

[0030] In like manner, a null may be detected by looking for a change from decreasing values of the envelope 128b to increasing values. For example, in Figure 4b, every change in frequency from f_6 or f_{12} results in a decrease in the envelope 128b. The change from f_{12} or f_{13}, however, causes the envelope 128b to increase. It can thus determined at step [[408]] 308 in Figure 3 that a null occurs at f_{12}, f_{13} , or at a frequency between f_{12} and f_{13} (e.g., an average of f_{12} and f_{13}). Again, the smaller the increments between frequency steps in Figure 4b, the greater the accuracy. Null 404a in Figure 4a may be similarly detected (e.g., by examining the slope of the envelope to determine whether the envelope is increasing or decreasing at a particular frequency).

Please replace paragraph [0036] with the following amended paragraph:

[0036] As mentioned above, Figure 7 illustrates a simplified block diagram of an exemplary implementation of the analyzer 602. As shown, Figure 7 includes an analog-to-digital converter 702, a digital memory 706, and a processor 710. (As shown in Figure 7, connector 704 connects analog-to-digital converter 702 and memory 706, and connector 708 connects memory 706 and processor 710.) Note that, if the envelope wave output 128 by envelope detector 122 is already in digital format (e.g., the envelope wave 128b in Figure 4b and Figure 5b), analog-to-digital converter may not be needed. Memory 706 may be any type of digital memory, including silicon based memories, magnetic based memories, optical based memories, etc. Processor 710 is preferably a microprocessor that operates under control of software (e.g., software, firmware, microcode, etc.) that resides in memory [[614]] 706. Alternatively, processor may consist in part or in whole of hardwired logic circuits.

Please replace paragraph [0045] with the following amended paragraph:

[0045] As shown in Figure 10, an analyzer 1050a, 1050b, and 1050c is associated with each of the communications channels 1060a, 1060b, and 1060c. Each analyzer 1050a, 1050b, and 1050c may be similar to a combination of the envelope detector 122 and analyzer 602 shown in Figure 6, and each analyzer 1050a, 1050b, and 1050c may execute a process similar to the process shown in Figure 8 to calculate the propagation delay through its associated channel 1060a, 1060b, and 1060c. (Each analyzer 1050a, 1050b, and 1050c may communicate with signal generator 1002 via bus 1070. As shown in Figure 10, connectors 1052a, 1052b, and 1052c connect each analyzer 1050a, 1050b, and 1050c to bus 1070.) Each analyzer 1050a, 1050b, and 1050c may communicate the calculated propagation delay of its associated communications channel 1060a, 1060b, or 1060c to an automatic calibration module 1022 (again communicating through bus 1070). Automatic calibration module 1022 may then set a variable delay module 1030a, 1030b, and 1030c in each channel 1060a, 1060b, and 1060c so that the overall propagation delay through each of the channels 1060a, 1060b, and 1060c is the same or within a specified tolerance. (As shown in Figure 10, automatic calibration module 1022 is connected to bus 1070, and connectors 1054a, 1054b, and 1054c connect variable delay modules 1030a, 1030b, and 1030c to bus 1070.) Variable delay modules 1030a, 1030b, and 1030c may be implemented in any suitable fashion. For example, these modules may be implemented as described in U.S. patent application serial no. 10/006,178, filed by Miller on December 4, 2001, and entitled "Adjustable Delay Transmission Line," which is incorporated by reference herein in its entirety. As another example, these modules may be implemented by delaying input of a signal to a driver 1006a, 1006b, or 1006c. As another example, the tester 902 may maintain offset tables for varying starting a test signal on a particular channel in order to compensate for variations in the propagation delays through the channels.